Amendments to the Claims

Please amend claims 21, 38 and 48 as shown below.

Listing of Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-20 (Cancelled).

21. (Currently amended) A semiconductor component comprising:

an insulating layer disposed on a semiconductor substrate; and

a capacitance structure formed in the insulating layer, the structure having two capacitance surface parts,

the first capacitance surface part having at least a first metallization plane and a second metallization plane extending approximately parallel to the substrate surface and are each operatively connected to one of two electrodes, and

the second capacitance surface part having at least one electrically conductive region between the first metallization plane and the second metallization plane in the insulating layer and is operatively connected to one of the first metallization plane and the second metallization plane where the second capacitance part is in the form of a homogeneous cohesive elevation, wherein the elevation comprises a top wall and side walls, wherein the top wall is oriented perpendicular to the side walls and wherein the side walls and the top wall are ~~an end which is surrounded by the insulating layer, and wherein the end of the elevation comprises a top portion which is~~ covered by the insulating layer.

22. (Previously presented) The semiconductor component of claim 21, where the electrically conductive region of the second capacitance part is produced with a Damascene process.

23. (Previously presented) The semiconductor component of claim 21, where the electrically conductive region of the second capacitance part is arranged at about a right angle to the first metallization plane and the second metallization plane.

24. (Previously presented) The semiconductor component of claim 21, where the electrically conductive region is divided into at least two parts, a first conductive region and a second conductive region and the first conductive region is operatively connected to the first metallization plane and the second conductive region is operatively connected to the second metallization plane.

25. (Previously presented) The semiconductor component of claim 24, where the metallization planes are in the form of a cohesive plate.

26. (Previously presented) The semiconductor component of claim 24, where the first conductive region further comprises a first plurality of conductive bar forms and the second conductive region further comprises a second plurality of conductive bar forms.

27. (Previously presented) The semiconductor component of claim 26, where the first plurality of bar forms are arranged at a fixed distance from one another on the first metallization plane and extend in the direction of the second metallization plane, and the second plurality of bar forms are arranged at a fixed distance from one another on the second metallization plane and extend in the direction of the first metallization plane.

28. (Previously presented) The semiconductor component of claim 27, where the first plurality of bar forms has a first length and the second plurality of bar forms has a second length and the first length is greater than, less than or the same length as the second length and the sum of the first length and the second length is greater than a distance between the first metallization plane and the second metallization plane.

29. (Previously presented) The semiconductor component of claim 21, where at least one of the first metallization plane and the second metallization plane is each comprised of at least two electrical lines in parallel to one another and the electrical lines of the first metallization

plane are arranged congruently with respect to the electrical lines of the second metallization plane.

30. (Previously presented) The semiconductor component of claim 29, where the electrically conductive region is divided into at least two parts, a first conductive region and a second conductive region, and the first conductive region is operatively arranged on the electrical lines of the first metallization plane and the second conductive region is operatively arranged on the electrical lines of the second metallization plane.

31. (Previously presented) The semiconductor component of claim 30, where the first conductive region further comprises a first plurality of conductive bar forms and the second conductive region further comprises a second plurality of conductive bar forms.

32. (Previously presented) The semiconductor component of claim 31, where the first plurality of bar forms are arranged at a fixed distance from one another on the electrical lines of the first metallization plane and extend in the direction of the second metallization plane, and the second plurality of bar forms are arranged at a fixed distance from one another on the electrical lines of the second metallization plane and are offset from the bars of the first conductive region and extend between the bars of the first conductive region in the direction of the first metallization plane.

33. (Previously presented) The semiconductor component of claim 32, where the first plurality of bar forms has a first length and the second plurality of bar forms has a second length and the first length is greater than, less than or the same length as the second length and the sum of the first length and the second length is greater than a distance between the first metallization plane and the second metallization plane.

34. (Previously presented) The semiconductor component of claim 21, where the first metallization plane is in the form of a cohesive plate and the second metallization plane is a lattice.

35. (Previously presented) The semiconductor component of claim 34, where the electrically conductive region is operatively attached to the first metallization plane and further

comprises a plurality of bar forms extending in the direction of the second metallization plane and at least one bar of the plurality of bars projects at least partially into a cutout in the lattice.

36. (Previously presented) The semiconductor component of claim 34, further comprising a third metallization plane in a form of a lattice and arranged parallel to and at a distance from the second metallization plane and the second and third metallization planes are electrically connected to one another.

37. (Previously presented) The semiconductor component of claim 36, where at least one of a plurality of bar forms project through the cut-out in the second metallization plane and extend at least partially into a cut-out in the third metallization plane.

38. (Currently amended) A method for fabricating a semiconductor component comprising:

disposing an insulator layer on a semiconductor substrate;

forming a first capacitance part in the insulating layer having at least a first metallization plane and a second metallization plane which are formed essentially parallel to the substrate surface; and

forming a second capacitance part that is an electrically conductive region that is homogeneous in the insulating layer between the metallization planes, where the electrically conducting region is operatively connected to one of the metallization planes, where the second capacitance part is in the form of a homogeneous cohesive elevation, wherein the elevation comprises a top wall and side walls, wherein the top wall is oriented perpendicular to the side walls and wherein the side walls and the top wall are ~~an end which is surrounded by the insulating layer, and wherein the end of the elevation comprises a top portion which is~~ covered by the insulating layer.

39. (Previously presented) The method of claim 38, further comprising forming the electrically conductive region in a homogeneous cohesive elevation, the region being formed between at least two metallization planes is formed by patterning the metallization plane.

40. (Previously presented) The method of claim 39, further comprising forming the electrically conductive region in the insulating material as a via structure.

41. (Previously presented) The method of claim 40, where the via structure arranges the electrically conductive region at essentially a right angle to the metallization planes.

42. (Previously presented) The method of claim 39, where the via structures form bars that are operatively connected to the first metallization plane extending towards the second metallization plane.

43. (Previously presented) The method of claim 38, further comprising forming the first metallization plane and the second metallization plane as a cohesive plate.

44. (Previously presented) The method of claim 38, further comprising forming the first metallization plane as at least two electrical lines arranged in parallel to one another and the second metallization plane as at least two electrical lines parallel to one another and the electrical lines of the first metallization plane are congruently arranged with respect to the electrical lines of the second metallization plane.

45. (Previously presented) The method of claim 38, further comprising forming the first metallization plane as a cohesive plate and the second metallization plane as a lattice plate.

46. (Previously presented) The method of claim 45, further comprising forming a third metallization plane formed as a lattice.

47. (Previously presented) The method of claim 46, further comprising forming a via arrangement that forms a bar extending from the first metallization plane through a cutout of the second metallization plane and extending into a cutout in the third metallization plane.

48. (Currently amended) A semiconductor component comprising:
an insulating layer disposed on a semiconductor substrate; and
a capacitance structure formed in the insulating layer,

a first metallization plane and a second metallization plane, said first and second metallization planes extending approximately parallel to the substrate surface, wherein

the capacitance structure comprises at least one electrically conducting element in the first metallization plane and at least one electrically conducting element in the second metallization plane, and at least one electrically conductive region between the first metallization plane and the second metallization plane in the insulating layer, the electrically conductive region being connected to one of the electrically conducting elements, and the electrically conductive region being in the form of a homogeneous cohesive elevation, wherein the elevation comprises a top wall and side wall, wherein the top wall is oriented perpendicular to the side walls and wherein the side walls and the top wall are ~~comprising an end which is surrounded by the insulating layer, and wherein the end of the elevation comprises a proximate portion which is electrically coupled with the one of the electrically conducting elements and a distal portion which is~~ covered by the insulating layer.